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RareBooksClub. Paperback. Book Condition: New. This item is printed on demand. Paperback. 32 pages. Original publisher: Washington, DC : National Aeronautics and Space Administration, 1992 OCLC Number: (OCoLC)645473355 Subject: Motherboards (Microcomputers) Excerpt: . . . LAR 14785-1-13-PATENT APPLICATION Figure 3 is a block diagram of a processing module 24, which is connected to RMU 1 through a read bus 25 and a write bus 26. The fiber optic cables of read bus 25 in processing module 24 correspond with the fiber optic cables of read bus 2 of RMU 1. The fiber optic cable of write bus 26 5 corresponds with one of the fiber optic cables of write bus 3 of RMU 1. As discussed above, the read bus 25 may be replicated to increase reliability. If it is, the replicated optical signals are passed through an optical combiner 27 and then a threshold enforcing receiver 28. Receiver 28 converts the optical signals to electronic signals. In addition, receiver 28 is threshold enforcing and 10 thus allows a majority of good optical signals to overwhelm a minority of erroneous optical signals. This is only possible if the optical signals are tightly synchronized, which they are because they are produced using a single time base in RMU 1. The data stream from receiver 28 is fed to a PLL 29, a clock synchronization unit 30 and a scheduler processor 32. PLL 29 locks its clock 15 with the data stream, thus regenerating the time base of RMU 1. The regenerated time base is fed to an optical transmitter 35 and the clock synchronization unit 30. Because the transmitter 35 of each local processing module 24 is driven by the clock derived by PLL 29, the transmitter 35 of each local processing module 24 is synchronized. Thus, data from each local...

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